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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference BUR920020082	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US02/41182	International filing date *(day/month/year)* 20 December 2002 (20.12.2002)	Priority date *(day/month/year)*
International Patent Classification (IPC) or national classification and IPC IPC(7): H01L 21/82, 21/44 and US Cl.: 438/131		
Applicant INTERNATIONAL BUSINESS MACHINES CORPORATION		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 3 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
20 July 2004 (20.07.2004)	12 April 2005 (12.04.2005)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/ US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Jennifer M. Kennedy Telephone No. (703) 308-0956

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US02/41182

I. Basis of the report

1. With regard to the elements of the international application:*

☐ the international application as originally filed.

☒ the description:
pages 1-7 as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the claims:
pages NONE, as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages 8-10, filed with the letter of 28 January 2005 (28.01.2005)

☒ the drawings:
pages 1-10, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☐ the description, pages NONE

☒ the claims, Nos. 2, 12

☐ the drawings, sheets/~~fig~~ NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as " originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*
*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US02/41182

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims 1, 3-11, 13-19	YES
	Claims NONE	NO
Inventive Step (IS)	Claims 1, 3-11, 13-19	YES
	Claims NONE	NO
Industrial Applicability (IA)	Claims 1, 3-11, 13-19	YES
	Claims NONE	NO

2. CITATIONS AND EXPLANATIONS

Claims 1, 3-11, and 13-19 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the method of oxidizing the exposed corners to form an oxide thereon, and removing the oxide formed in said oxidizing step prior to said step of forming an oxide layer or wherein an oxide layer on the semiconducting material and overlying the corners, and the elongated tips are formed by oxidation of the exposed corners, the oxide formed thereby being different from the oxide layer.

Claims 1, 3-11, and 13-19 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.

Claims

1. A method for fabricating an antifuse structure (100) integrated with a semiconductor device, the method comprising the steps of:

forming a region of semiconducting material (11) overlying an insulator (3) disposed on a substrate (10);

performing an etching process to expose a plurality of corners (111-114) in the semiconducting material;

forming a plurality of elongated tips (111t, 112t, 113t, 114t) of the semiconducting material at the respective corners by oxidizing the exposed corners (111, 112, 113, 114) to form an oxide (31) thereon and then removing the oxide (31);

subsequently forming an oxide layer (51) on the semiconducting material and overlying the corners, the oxide layer having a nominal thickness and a reduced thickness at the corners less than the nominal thickness; and

forming a layer of conducting material (60) in contact with the oxide layer (51) at the corners,

thereby forming a plurality of possible breakdown paths at said corners, between the semiconducting material and the layer of conducting material through the oxide layer.

3. A method according to claim 1, characterized in that the region of semiconducting material (11) is a fin formed in a FINFET process.

4. A method according to claim 1, characterized in that the region of semiconducting material (211) is a gate region formed in a planar CMOS process.

5. A method according to claim 3 or claim 4, further comprising the step of doping the region of semiconducting material (11, 211).

6. A method according to claim 1, characterized in that oxidizing the exposed corners is performed in accordance with a low-temperature oxidation process.

7. A method according to any preceding claim, characterized in that the breakdown paths are electrically in parallel.

8. A method according to any preceding claim, further comprising the step of applying a voltage to the antifuse structure, thereby converting at least one of the breakdown paths to a conducting path (103, 280) through the oxide layer (51, 251).

9. A method according to claim 8, characterized in that the voltage is applied in accordance with a burn-in process for the device.

10. A method according to claim 8, characterized in that the device has a nominal voltage, and the applied voltage is approximately 1.5 times the nominal voltage.

11. An antifuse structure (100) integrated with a semiconductor device, the structure comprising:

a region of semiconducting material (11) overlying an insulator (3) disposed on a substrate (10), the semiconducting material having a plurality of corners (111-114) with a plurality of elongated tips (111t, 112t, 113t, 114t) of the semiconducting material at the respective corners;

an oxide layer (51) on the semiconducting material and overlying the corners and in contact with the corners, the oxide layer having a nominal thickness and a reduced thickness at the corners less than the nominal thickness; and

a layer of conducting material (60) in contact with the oxide layer (51) at the corners,

characterized in that

a plurality of possible breakdown paths are disposed at said corners, between the semiconducting material and the layer of conducting material through the reduced thickness of the oxide layer, and

the elongated tips are formed by oxidation of the exposed corners (111, 112, 113, 114), the oxide formed thereby being different from the oxide layer (51).

13. An antifuse structure according to claim 11, characterized in that the region of semiconducting material (11) is a fin formed in a FINFET process.

14. An antifuse structure according to claim 11, characterized in that the region of semiconducting material (211) is a gate region formed in a planar CMOS process.

15. An antifuse structure according to claim 11, characterized in that the region of semiconducting material (11, 211) is a region of doped material.

16. An antifuse structure according to any preceding claim, characterized in that the breakdown paths are electrically in parallel.

17. An antifuse structure according to any preceding claim, characterized in that at least one of the breakdown paths is a conducting path (103, 280) through the oxide layer (51, 251) formed by application of a voltage thereto.

18. An antifuse structure according to claim 17, characterized in that the applied voltage is a burn-in voltage for the device.

19. An antifuse structure according to claim 18, characterized in that the device has a nominal voltage, and the applied voltage is approximately 1.5 times the nominal voltage.